

CLAIMS

What is claimed is:

- Sub A2
- 1 1. A method of reducing interference in a circuit having a PLL, wherein the circuit is
2 formed on an integrated circuit, the method comprising the steps of:
3 providing a divider circuit at the input of the PLL for dividing the frequency of an input
4 signal by a desired amount; and
5 providing the divider circuit by placing a fixed-value divider at the input of the PLL to
6 reduce the digital current created by the PLL.

- Sub B1
- 1 2. The method of claim 1, wherein the step of providing a divider circuit further
2 comprises the step of providing first and second dividers connected in series at the input
3 of the PLL, wherein the first and second dividers are fixed-value dividers.

- 1 3. The method of claim 2, wherein the one of the dividers divides the input
2 frequency by thirteen and the other divider divides the input frequency by five.

- 1 4. The method of claim 1, wherein:
2 the PLL is powered by a first voltage;
3 the divider circuit is powered by a second voltage; and
4 the second voltage is less than the first voltage.

- Sub A3
- 1 5. A method of reducing interference present in a circuit comprising the step of:
2 reducing the mutual inductance between digital circuitry in a first portion of the circuit
3 and circuitry in a second portion of the circuit by placing a filter between the

4 digital circuitry and a voltage source external to the circuit in order to reduce the
5 area of a high frequency current loop.

1 ✓ 6. The method of claim 5, wherein the circuit is formed on an integrated circuit, and
2 wherein the first portion of the circuit includes PLL digital circuitry and the second
3 portion includes a VCO.

1 7. The method of claim 5, wherein the filter is a low pass filter.

1 8. The method of claim 5, wherein the filter creates a secondary current loop for
2 confining current at a desired frequency in the secondary current loop.

1 9. The method of claim 8, wherein the filter creates a third current loop for confining
2 current at a desired frequency in the third current loop.

1 ✓ 10. The method of claim 5, wherein the filter is provided by placing a capacitor
2 across first and second nodes in the digital circuitry and placing a resistor between the
3 first node and the voltage source.

1 11. The method of claim 10, wherein the filter is further provided by placing a second
2 capacitor between the second node and the resistor and placing a second resistor between
3 the first resistor and the voltage source.

1 12. A method of reducing interference present in a circuit formed on an integrated
2 circuit comprising the steps of:
3 identifying a conductive trace on the circuit carrying high frequency digital current; and

5 a contact connecting the conductive strip to a reference voltage.

1 20. The conduit of claim 19, wherein the contact is connected to the conductive strip
2 near an end of the conductive strip.

1 21. The conduit of claim 20, wherein the conductive strip is open at the opposite end.

1 22. The conduit of claim 19, further comprising a second conductive strip positioned
2 substantially parallel to the conductive trace.

1 23. The conduit of claim 22, wherein the first and second conductive strips are
2 positioned on opposite sides of the conductive trace.

1 24. The conduit of claim 19, wherein the circuit is an integrated circuit which
2 includes multiple metal layers, and wherein the conductive trace is formed on one of the
3 metal layers.

1 25. The conduit of claim 24, wherein the first conductive strip is formed on a first
2 metal layer.

1 26. The conduit of claim 25, further comprising a second conductive strip formed on
2 a second metal layer.

1 27. The conduit of claim 26, wherein the first and second conductive strips are
2 electrically connected together.

1 28. The conduit of claim 27, wherein the first and second conductive strips are
2 connected to the substrate of the integrated circuit.

1 29. The conduit of claim 19, wherein the integrated circuit includes PLL and VCO
2 circuitry for use with a wireless communications system.

1 30. A method of reducing interference present in a circuit, the circuit having a
2 plurality of similar circuit elements, the method comprising the step of:
3 forming at least some of the similar circuit elements on the circuit such that adjacent
4 circuit elements are mirror images of one another.

1 31. The method of claim 30, wherein the circuit is formed on an integrated circuit
2 having PLL and VCO circuitry for a wireless communications system.

1 32. The method of claim 30, wherein the circuit elements are flip flops.

1 33. The method of claim 32, wherein the flip flops form counters for the PLL.

1 34. A method of reducing interference present in a circuit, the method comprising the
2 steps of:
3 providing a first block of digital circuitry connected to a second block of digital circuitry
4 by a signal line; and
5 inserting buffer circuitry between the first and second blocks of digital circuitry for
6 containing high frequency current within the first block of digital circuitry.

1 35. The method of claim 34, wherein the circuit is formed on an integrated circuit
2 having PLL and VCO circuitry for a wireless communications system.

1 36. The method of claim 34, wherein the buffer circuitry is formed on an integrated
2 circuit near the location on the integrated circuit where the first block of digital circuitry
3 is formed.

1 37. The method of claim 34, wherein the signal line is a control line.

1 38. The method of claim 34, wherein the signal line is a status line.

1 39. The method of claim 34, wherein the buffer circuitry is comprised of one or more
2 inverters.

1 40. The method of claim 39, wherein at least one of the inverters is powered by a
2 filtering capacitor coupled to the at least one inverter.

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1 41. A method of reducing interference present in a circuit formed on an integrated
2 circuit having PLL and VCO circuitry, the method comprising the step of:
3 identifying circuitry in the circuit in which the impedance of the circuitry changes state
4 over time during operation of the circuit; and
5 creating replica circuitry of the identified circuitry which operates in a state opposite of
6 the identified circuitry.

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1 42. The method of claim 41, wherein the replicated circuitry has no function in the
2 circuit other than reducing interference.

1 43. The method of claim 41, wherein the identified circuitry is comprised of a first
2 inverter having a high state and a low state, wherein the replica circuitry is comprised of
3 a second inverter having a high state and a low state, and wherein the replica inverter is
4 controlled to be in the opposite state of the other inverter.

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1 44. The method of claim 41, wherein the replica circuitry is comprised of circuitry
2 similar to the identified circuitry, the method further comprising the step of connecting an
3 inverter between an input of the identified circuitry and an input of the replica circuitry.

1 45. A filter for filtering an interface pin of integrated circuit having PLL and VCO
2 circuitry to reduce interference caused by signals at the interface pin of the integrated
3 circuit, the filter comprising:
4 a filter coupled to the interface pin of the integrated circuit.

1 46. The filter of claim 45, wherein the interface pin is a clock signal input for
2 receiving a clock signal from an external clock source, and wherein the filter isolates the
3 clock signal while allowing the clock signal to pass through to the integrated circuit.

1 47. The filter of claim 46, wherein the filter is an RC filter.

1 54. The method of claim 53, wherein the divider circuitry further comprises first and
2 second series connected fixed dividers.

1 55. The method of claim 52, wherein the one or more techniques includes reducing
2 the mutual inductance between digital circuitry in the PLL and the VCO circuitry by
3 placing a filter between digital circuitry in the PLL and a voltage source external to the
4 integrated circuit in order to reduce the area of a high frequency current loop.

1 56. The method of claim 52, wherein the one of the one or more techniques includes:
2 identifying a conductive trace on the integrated circuit carrying high frequency digital
3 current; and
4 placing a conductive strip in the proximity of the identified conductive trace to help
5 contain the high frequency digital current flowing through the conductive trace.

1 57. The method of claim 52, wherein the integrated circuit includes a plurality of
2 similar circuit elements, and wherein one of the one or more techniques includes forming
3 at least some of the similar circuit elements on the integrated circuit such that adjacent
4 circuit elements are mirror images of one another.

1 58. The method of claim 52, wherein one of the one or more techniques includes
2 providing a first block of digital circuitry connected to a second block of digital circuitry
3 by a signal line, and inserting buffer circuitry between the first and second blocks of
4 digital circuitry for containing high frequency current within the first block of digital
5 circuitry.

1 59. The method of claim 52, wherein one of the one or more techniques includes the
2 steps of:
3 identifying circuitry in the integrated circuit in which the impedance of the circuitry
4 changes over time during operation of the integrated circuit; and
5 creating replica circuitry of the identified circuitry which operates in a phase opposite of
6 the identified circuitry.

1 60. The method of claim 52, wherein the integrated circuit includes an interface pin,
2 wherein one of the one or more techniques includes the step of:
3 providing a filter coupled to the interface pin of the integrated circuit to reduce
4 interference caused by signals at the interface pin.

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